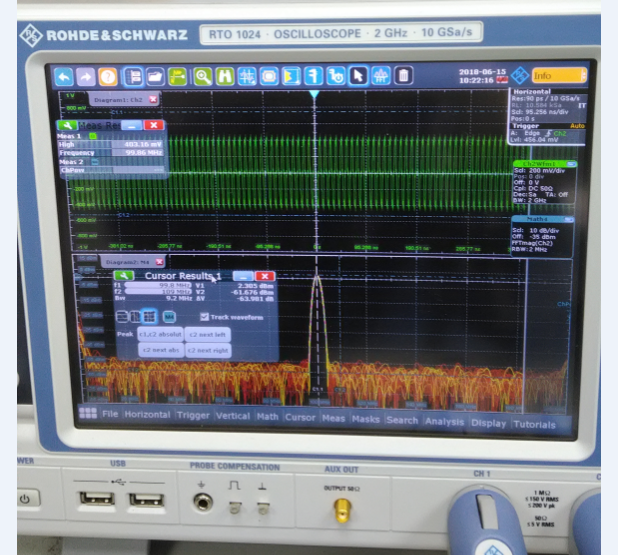
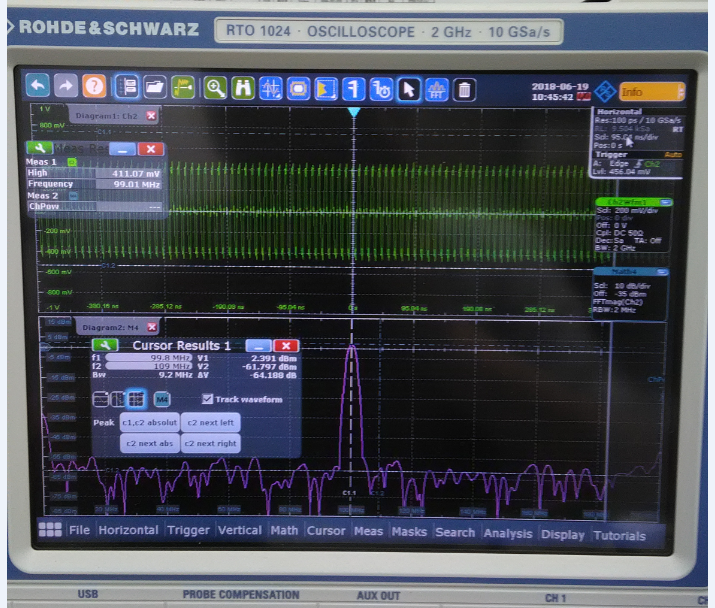
<https://devtalk.nvidia.com/default/topic/962847/?comment=4995007> **#13**  
drivers/platform/tegra/tegra21\_clocks.c  
  
#define USE\_PLLE\_SS 0  
  
  
  
#if USE\_PLLE\_SS  
val = clk\_readl(PLLE\_SS\_CTRL);  
val &= ~(PLLE\_SS\_CNTL\_CENTER | PLLE\_SS\_CNTL\_INVERT);  
val &= ~PLLE\_SS\_COEFFICIENTS\_MASK;  
val |= PLLE\_SS\_COEFFICIENTS\_VAL;  
clk\_writel(val, PLLE\_SS\_CTRL);  
val &= ~(PLLE\_SS\_CNTL\_SSC\_BYP | PLLE\_SS\_CNTL\_BYPASS\_SS);  
pll\_writel\_delay(val, PLLE\_SS\_CTRL);  
val &= ~PLLE\_SS\_CNTL\_INTERP\_RESET;  
pll\_writel\_delay(val, PLLE\_SS\_CTRL);  
#endif  
  
include/linux/platform/tegra/clock.h  
  
  
#ifdef CONFIG\_ARCH\_TEGRA\_2x\_SOC  
#define USE\_PLL\_LOCK\_BITS 0 /\* Never use lock bits on Tegra2 \*/  
#else  
#define USE\_PLL\_LOCK\_BITS 1 /\* Use lock bits for PLL stabiliation \*/  
#define USE\_PLLE\_SS 0 /\* Use spread spectrum coefficients for PLLE \*/  
#define PLL\_PRE\_LOCK\_DELAY 2 /\* Delay 1st lock bit read after pll enabled \*/  
#ifdef CONFIG\_ARCH\_TEGRA\_3x\_SOC  
#define PLL\_POST\_LOCK\_DELAY 50 /\* Safety delay after lock is detected \*/  
#else  
#define USE\_PLLE\_SWCTL 0 /\* Use s/w controls for PLLE \*/  
#define PLL\_POST\_LOCK\_DELAY 10 /\* Safety delay after lock is detected \*/  
#endif  
#endif

**Without** <https://devtalk.nvidia.com/default/topic/962847/?comment=4995007> **#13**

**With** <https://devtalk.nvidia.com/default/topic/962847/?comment=4995007> **#13**



# Result: no difference between above two waveforms when disable SSC (Spread Spectrum Clocking) PEX\_CLK0\_P & PEX\_CLK0\_N on Jetson TX1 Developer Kit.