For the settings of Left and Right ganged mode for Nvidia TX2, we compared the following setting under the same resolution of 3840 x 1080 @ 30fps using the DSI analyzer from Keysight M9505A

**1. Data lanes = 4, ganged type = 0**

**2. Data lanes = 8, ganged type = 1**

**For Data lanes = 4, ganged type = 0**

Following is the dsi node settings

dsi {

status = "ok";

panel-s-wqxga-10-1 {

status = "ok";

/\*\* Note these are just the values we're changing. See decompiled.dts for all values \*/

nvidia,dsi-instance = <0x2>; // 0x0 or 0x02 (For DSI-C

nvidia,dsi-pixel-format = <0x3>;

nvidia,dsi-refresh-rate = <30>; // orig = 60

nvidia,dsi-rated-refresh-rate = <60>;

nvidia,dsi-n-data-lanes = <0x4>; /\* orig = 0x8 \*/

nvidia,dsi-ganged-type = <0x0>; /\* 0, Not Ganged, 1 SYMMETRIC\_LEFT\_RIGHT\*/

nvidia,dsi-ganged-write-to-all-links = <0x1>; /\* ?? \*/

/\*\* The following seems missing from the original device tree \*/

nvidia,dsi-split-link-type = <0x0>;

nvidia,dsi-video-data-type = <0x0>; /\* VIDEO\_MODE (not COMMAND\_MODE) \*/

nvidia,dsi-video-clock-mode = <0x0>; /\* CLOCK MODE CONTINUOUS \*/

/\* nvidia,dsi-video-burst-mode = <0x3>; TEGRA\_DSI\_VIDEO\_BURST\_MODE\_LOW\_SPEED \*/

/\* nvidia,dsi-video-burst-mode = <0x0>; TEGRA\_DSI\_VIDEO\_NONE \*/

nvidia,dsi-video-burst-mode = <0x1>; /\* TEGRA\_DSI\_VIDEO\_NONE\_WITH\_SYNC\_END \*/

nvidia,dsi-power-saving-suspend = <0x0>;

disp-default-out {

nvidia,out-type = <0x2>;

nvidia,out-width = <0xd8>;

nvidia,out-height = <0x87>;

nvidia,out-flags = <0x00>; /\* Continious Mode?? (was 0x20 one shot LP Mode) \*/

nvidia,out-parent-clk = "pll\_d";

nvidia,out-xres = <3840>; /\* orig = 1920 \*/

nvidia,out-yres = <1080>; /\* orig = 1080 \*/

nvidia,out-rotation = <0>;

};

display-timings {

// double wide

3840x1080-32 {

clock-frequency = <278100000>; // was 148500000, doubled 297000000

hactive = <3840>; // orig = 1920 was 3840

vactive = <1080>; // orig = 1080

hfront-porch = <88>; // orig = 88

hback-porch = <148>; // orig = 148

hsync-len = <44>; // orig = 44

vfront-porch = <4>; // orig = 4

vback-porch = <36>; // orig = 36

vsync-len = <5>; // orig = 5

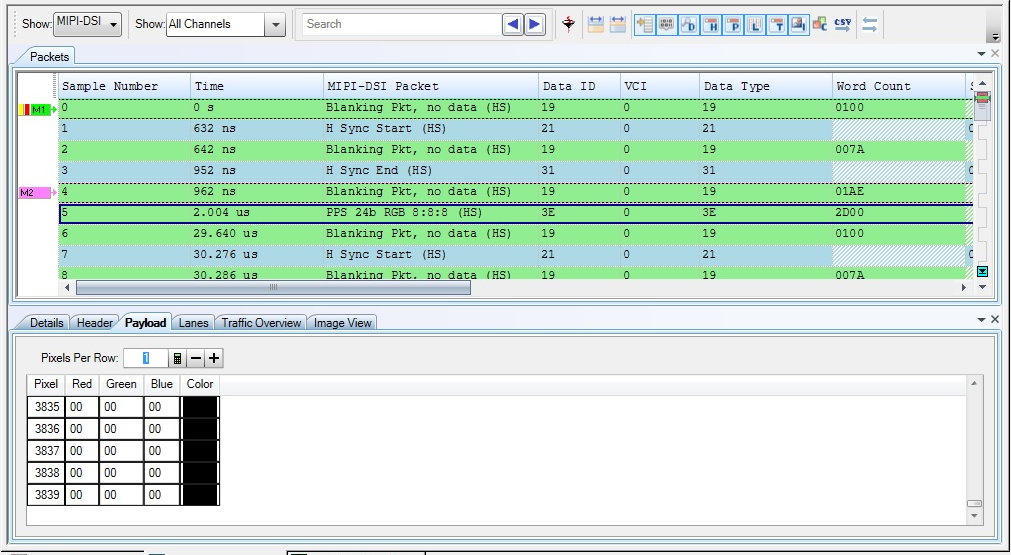
nvidia,h-ref-to-sync = <1>;

nvidia,v-ref-to-sync = <1>;

};

Note that after starting the TX2 we ran Xorg, an xterm (to keep the display from blanking) and ran “xsetroot -solid green” to set the background of the raster to green.

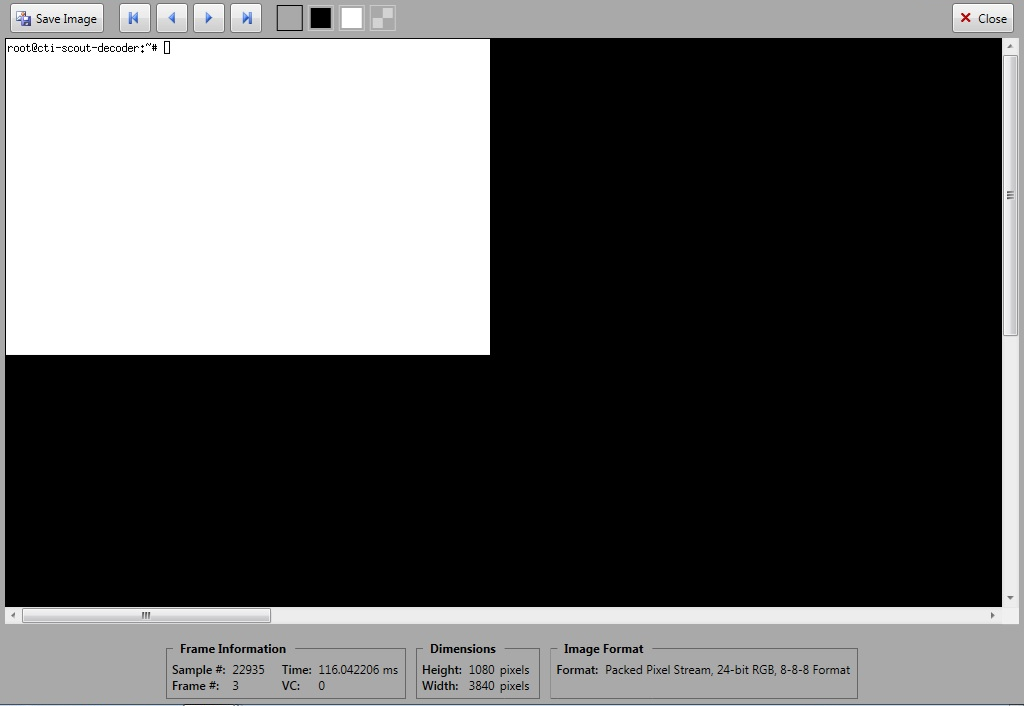
Pic 1



Picture 1 from analyzer show the correct line sequence with H Sync Start, Blanking, and H Sync End for the Horizontal sync pulse. Then blanking for the back porch and 24 bit RGB data and blanking for the front porch. All packets have correct word count according to the dsi node settings

Also number of pixels per packet per line match with the dsi node settings of 3840 pixels (bottom window)

Pic 2



Picture 2 from analyzer show the actual display image with correct Dimension listed at the bottom of 3840 x 1080 that match with the dsi settings.

**For Data lanes = 8, ganged type = 1**

Following is the dsi node settings

dsi {

status = "ok";

panel-s-wqxga-10-1 {

status = "ok";

/\*\* Note these are just the values we're changing. See decompiled.dts for all values \*/

nvidia,dsi-instance = <0x2>; // 0x0 or 0x02 (For DSI-C

nvidia,dsi-pixel-format = <0x3>;

nvidia,dsi-refresh-rate = <30>; // orig = 60

nvidia,dsi-rated-refresh-rate = <60>;

nvidia,dsi-n-data-lanes = <0x8>; /\* orig = 0x8 \*/

nvidia,dsi-ganged-type = <0x1>; /\* 0, Not Ganged, 1 SYMMETRIC\_LEFT\_RIGHT\*/

nvidia,dsi-ganged-write-to-all-links = <0x1>; /\* ?? \*/

/\*\* The following seems missing from the original device tree \*/

nvidia,dsi-split-link-type = <0x0>;

nvidia,dsi-video-data-type = <0x0>; /\* VIDEO\_MODE (not COMMAND\_MODE) \*/

nvidia,dsi-video-clock-mode = <0x0>; /\* CLOCK MODE CONTINUOUS \*/

/\* nvidia,dsi-video-burst-mode = <0x3>; TEGRA\_DSI\_VIDEO\_BURST\_MODE\_LOW\_SPEED \*/

/\* nvidia,dsi-video-burst-mode = <0x0>; TEGRA\_DSI\_VIDEO\_NONE \*/

nvidia,dsi-video-burst-mode = <0x1>; /\* TEGRA\_DSI\_VIDEO\_NONE\_WITH\_SYNC\_END \*/

nvidia,dsi-power-saving-suspend = <0x0>;

disp-default-out {

nvidia,out-type = <0x2>;

nvidia,out-width = <0xd8>;

nvidia,out-height = <0x87>;

nvidia,out-flags = <0x00>; /\* Continious Mode?? (was 0x20 one shot LP Mode) \*/

nvidia,out-parent-clk = "pll\_d";

nvidia,out-xres = <3840>; /\* orig = 1920 \*/

nvidia,out-yres = <1080>; /\* orig = 1080 \*/

nvidia,out-rotation = <0>;

};

display-timings {

// double wide

3840x1080-32 {

clock-frequency = <278100000>; // was 148500000, doubled 297000000

hactive = <3840>; // orig = 1920 was 3840

vactive = <1080>; // orig = 1080

hfront-porch = <88>; // orig = 88

hback-porch = <148>; // orig = 148

hsync-len = <44>; // orig = 44

vfront-porch = <4>; // orig = 4

vback-porch = <36>; // orig = 36

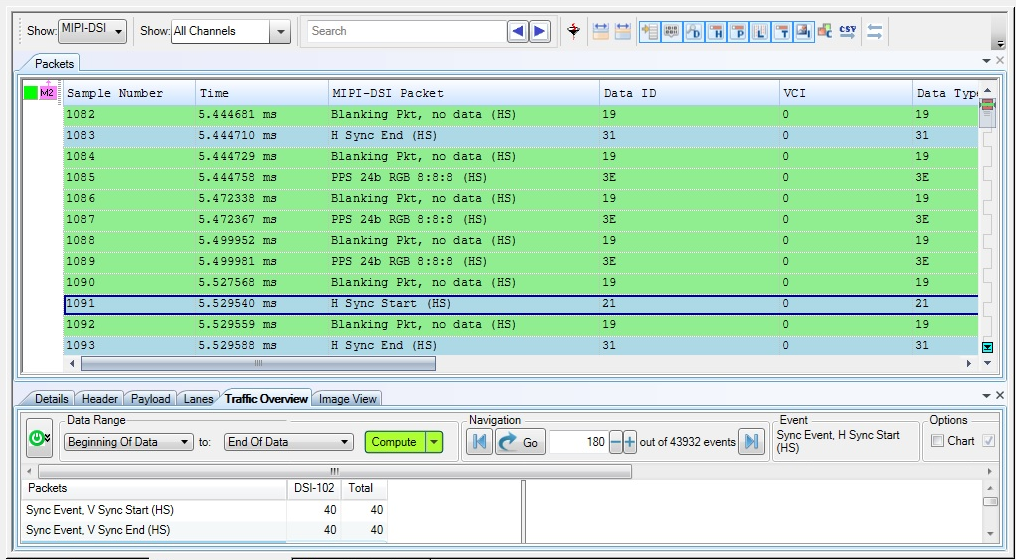
vsync-len = <5>; // orig = 5

nvidia,h-ref-to-sync = <1>;

nvidia,v-ref-to-sync = <1>;

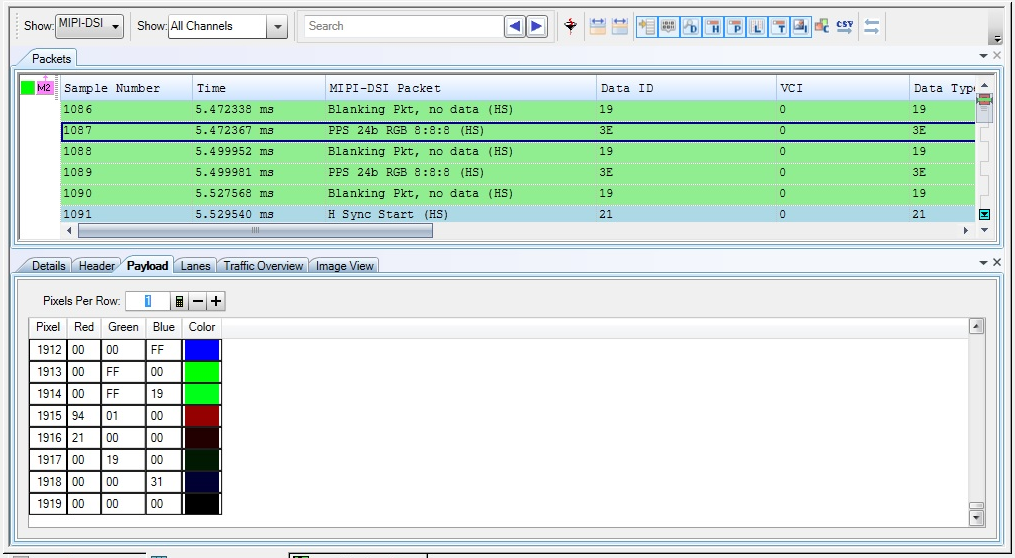
};

Pic 3



Picture 3 from the analyzer show missing H Sync Start and H Sync End packet from the TX2 DSI for 2 lines (sample 1086 and sample 1088) under the lane 8 , ganged mode 1 setting

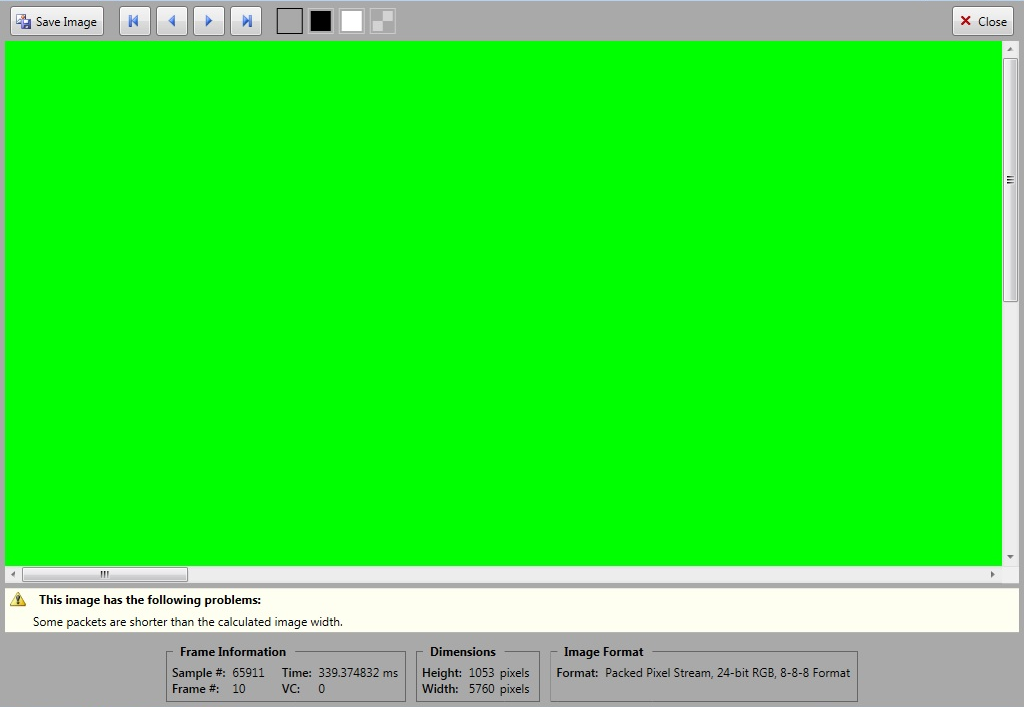
Pic 4



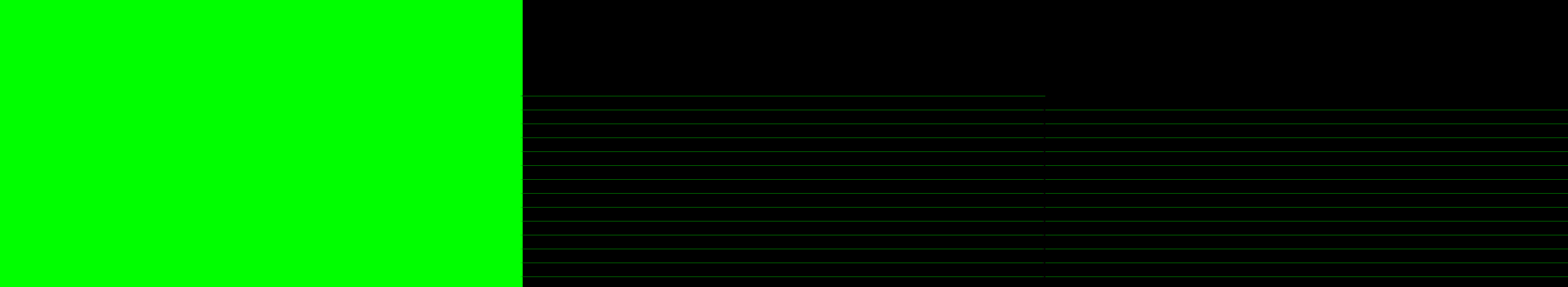
Picture 4 from analyzer show number of pixels per packet per line is 1920 which is half of the 3840 and that what we plan to output on each DSI under the Left and Right ganged mode. However when it compared to the video output from the analyzer (Pic 5) the width number are different. Also the height and width number compare to the dsi node settings are also different. Note the error message that says “some packets are shorter than the calculated image width”

IMPORTANT: this is just the upper left corner of the image. The entire image is available, but it looks like PIC 5b

Pic 5



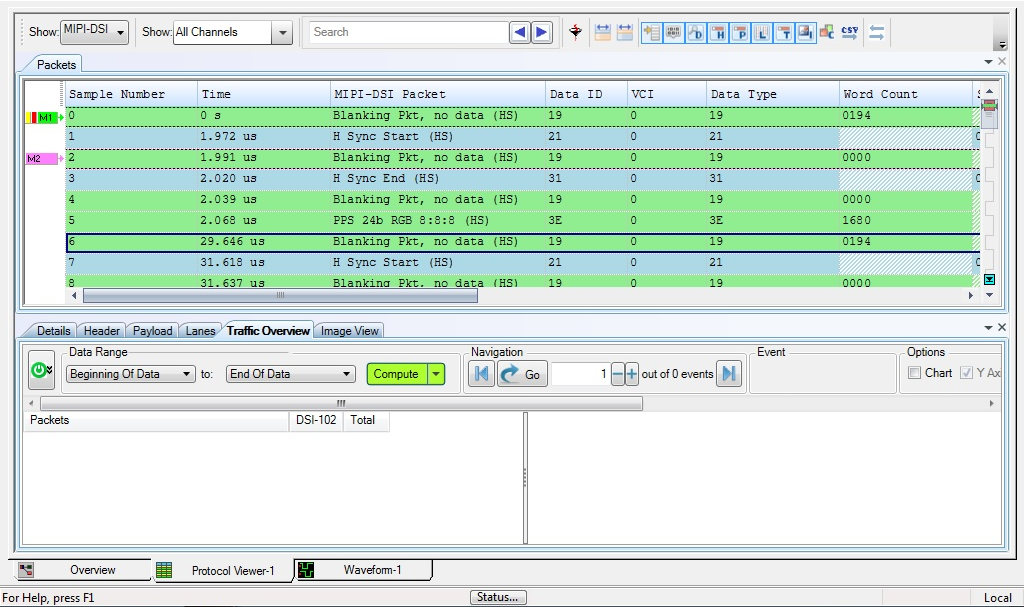
Pic 5B



Note that what may not be visible is that there are periodic green lines across the right (black) two thirds of the image.

What we believe is happening is that when the horizontal sync packets are missing, the analyzer continues with the current line. Periodically there are 3 data packets between sync packets, as shown in figure three, resulting in some of the scan lines being 3 times two wide, and the image captured by the analyzer gets stretched out.

Pic 6



Pic 6 show the blanking packet between the H Sync Start and End is 0 and Back porch blanking is also 0. The pixel count is 1680h = 5760 / 3 bytes per pixel = 1920. The front porch is 194h = 404 / 3 = 134 that not match with the horizontal front porch setting in the dsi node.

So in conclusion that when the dsi node setup for Lane = 8 and ganged mode of 1 (Left and right mode) the TX2 DSI output does not follow the line settings from the dsi node. It output missing Horizontal sync start and sync end packets in some lines. Also at the packet protocol analyzer the number of pixels per line are different between the packages and the actual image.

Note that we are also getting an overflow error message like this

tegradc 15200000.nvdisplay: dsi: video fifo overflow. Resetting flag

Which indicates a line buffer overflow.

One suspicion we have is that there is a timing mismatch between the dc and the dsi modules, causing an overflow, causing the horizontal sync packets to be lost. We believe that some of the dc or dsi registers may be being set to incorrect values for ganged mode.